FIG. 1

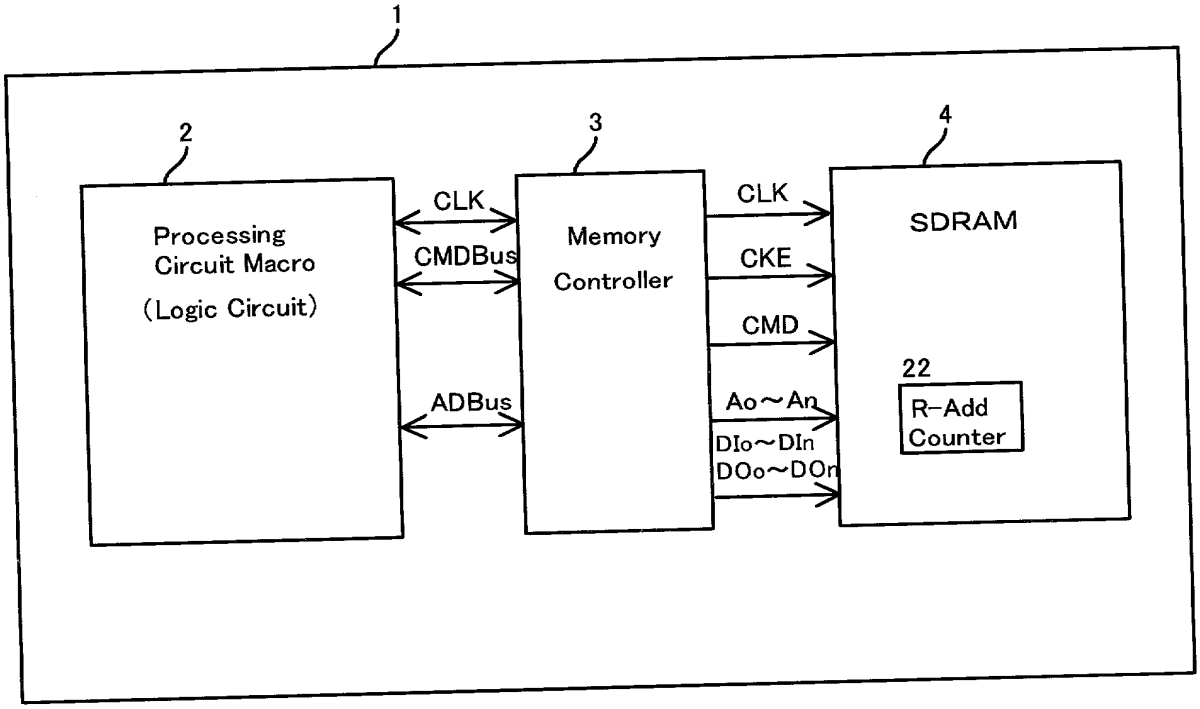
1
2
3
4
Processing
Circuit Macro
(Logic Circuit)
CLK
CMDBus
ADBus
Memory
Controller
CLK
CKE
CMD
Ao～An
DIo～DIn
DOo～DOn
SDRAM
22
R-Add
Counter

FIG. 2

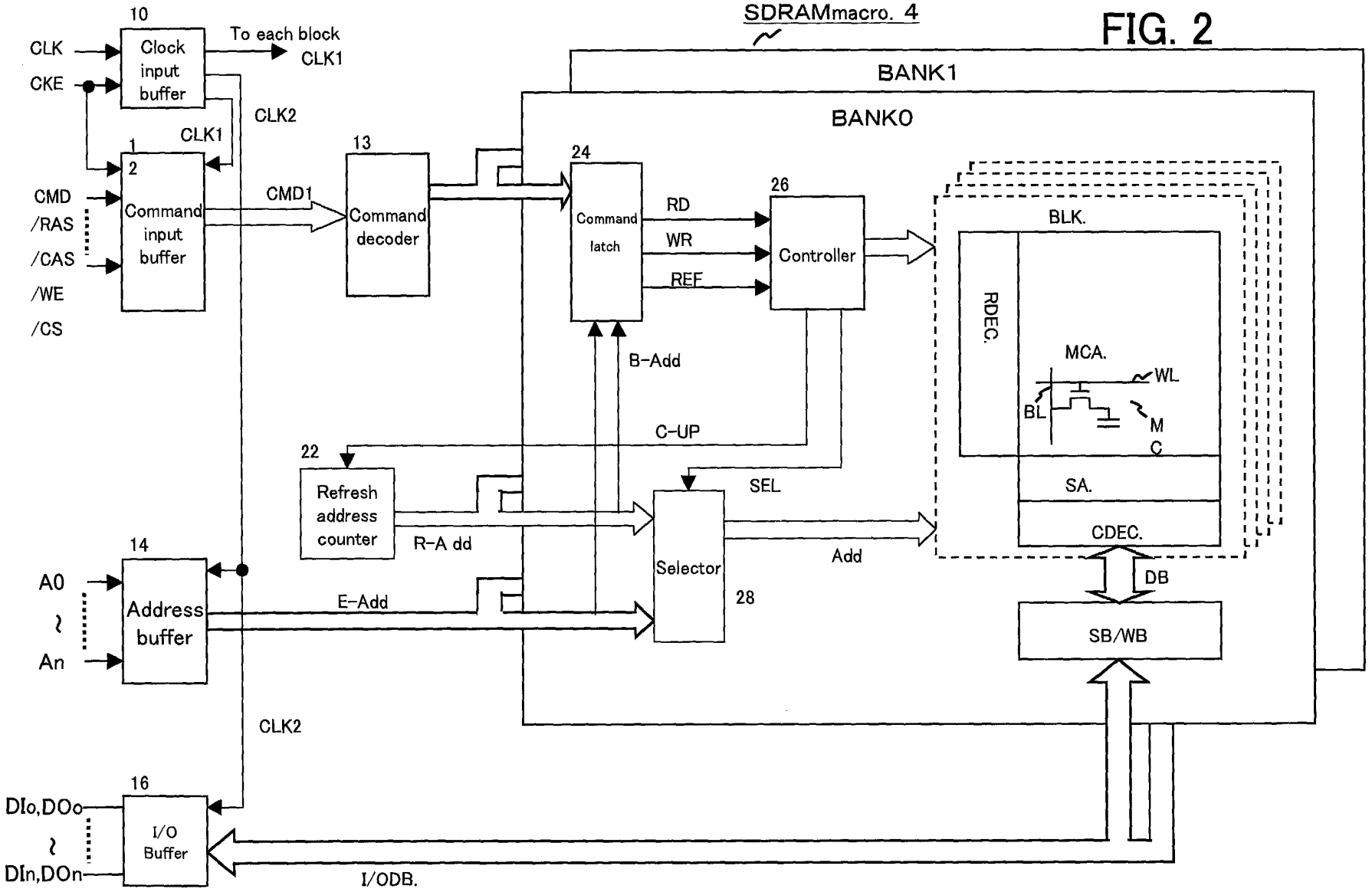
SDRAMmacro. 4
BANK1
BANK0
10
Clock input buffer
CLK
CKE
To each block
CLK1
CLK2
1
2
Command input buffer
CMD
/RAS
/CAS
/WE
/CS
CLK1
CMD1
13
Command decoder
24
Command latch
RD
WR
REF
26
Controller
B-Add
C-UP
22
Refresh address counter
R-A dd
SEL
Selector
28
Add
E-Add
14
Address buffer
A0
An
CLK2
16
I/O Buffer
DIo,DOo
DIn,DOn
I/ODB.
BLK.
RDEC.
MCA.
WL
BL
M
C
SA.
CDEC.
DB
SB/WB

FIG. 3

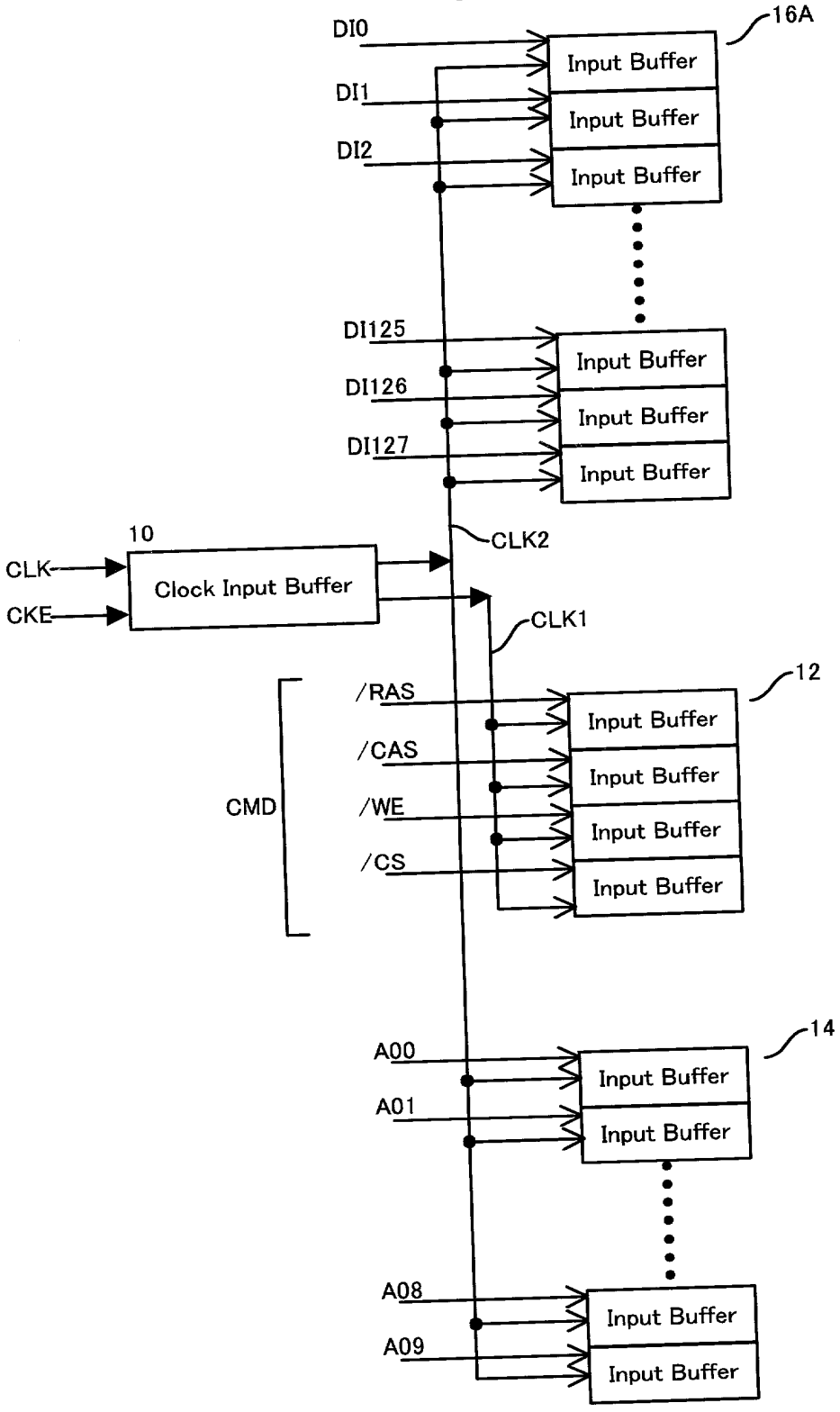
16A
DI0
DI1
DI2
Input Buffer
Input Buffer
Input Buffer
DI125
DI126
DI127
Input Buffer
Input Buffer
Input Buffer
10
CLK
CKE
Clock Input Buffer
CLK2
CLK1
12
CMD
/RAS
/CAS
/WE
/CS
Input Buffer
Input Buffer
Input Buffer
Input Buffer
14
A00
A01
A08
A09
Input Buffer
Input Buffer
Input Buffer
Input Buffer

FIG. 4

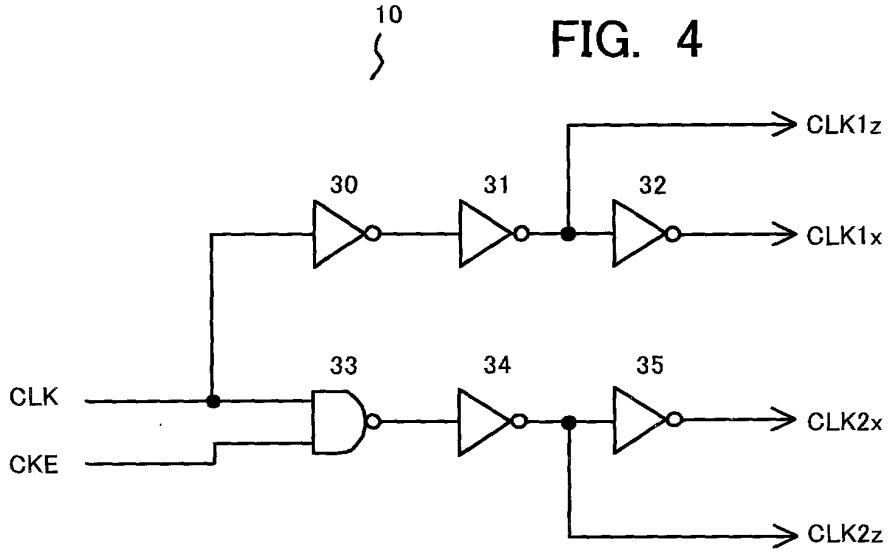

FIG. 5

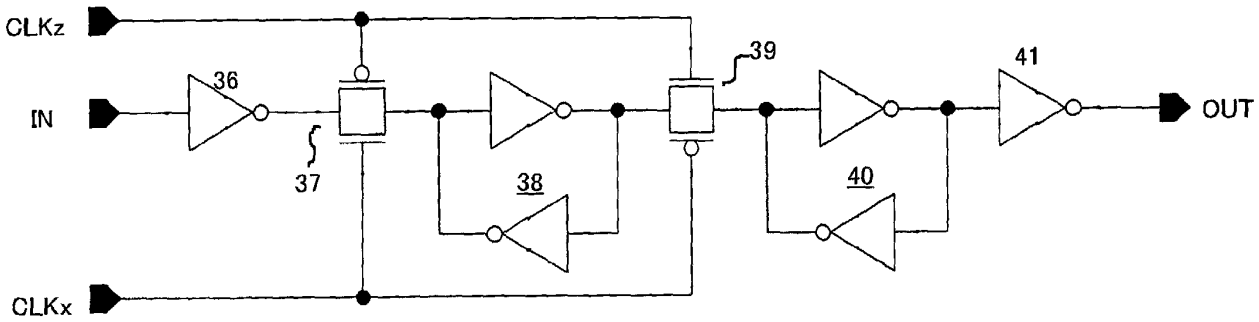

FIG. 6

CKE	Operation mode	Clock
H	Normal operation	CLK1 CLK2
L	Power down (Refresh entry mode)	CLK2

FIG. 7

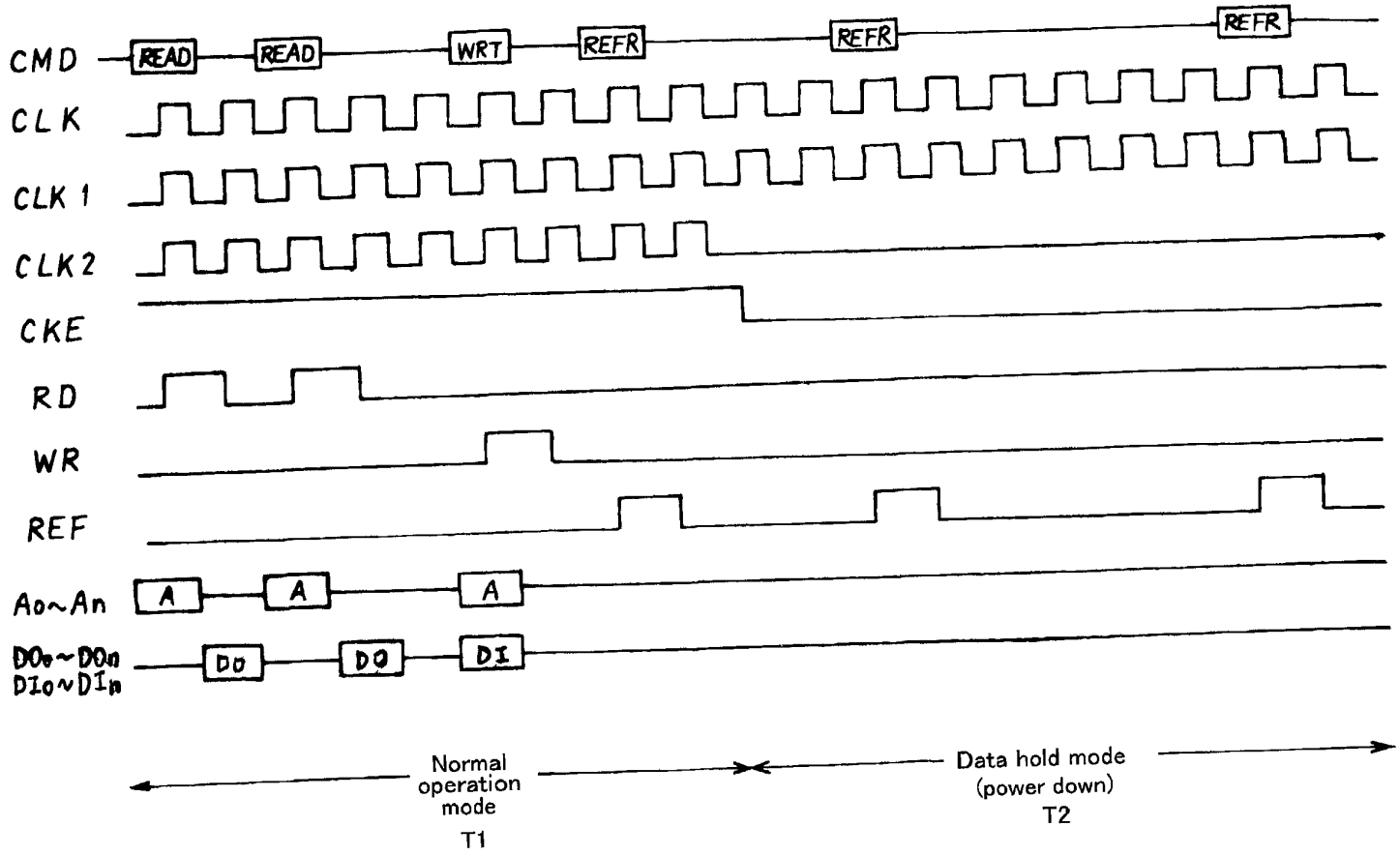
CMD
READ
READ
WRT
REFR
REFR
REFR
CLK
CLK1
CLK2
CKE
RD
WR
REF
A0~An
A
A
A
DQ0~DQn
DI0~DIn
DQ
DQ
DI
Normal operation mode
T1
Data hold mode (power down)
T2

FIG. 8

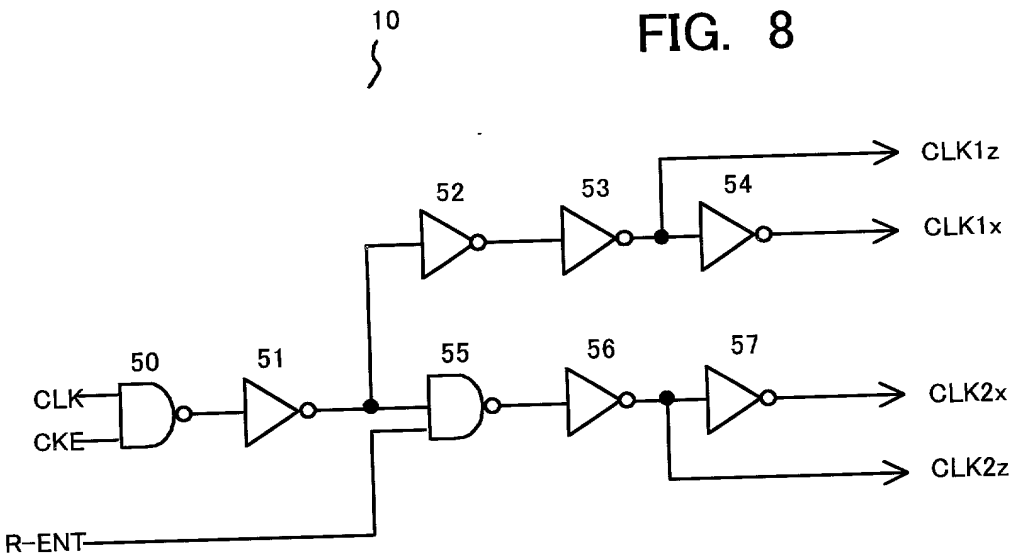

FIG. 9

CKE	R-ENT	Operation mode	Clock
H	H	Normal operation	CLK1 CLK2
H	L	Refresh entry mode	CLK1
L	—	Power down	—

FIG. 10

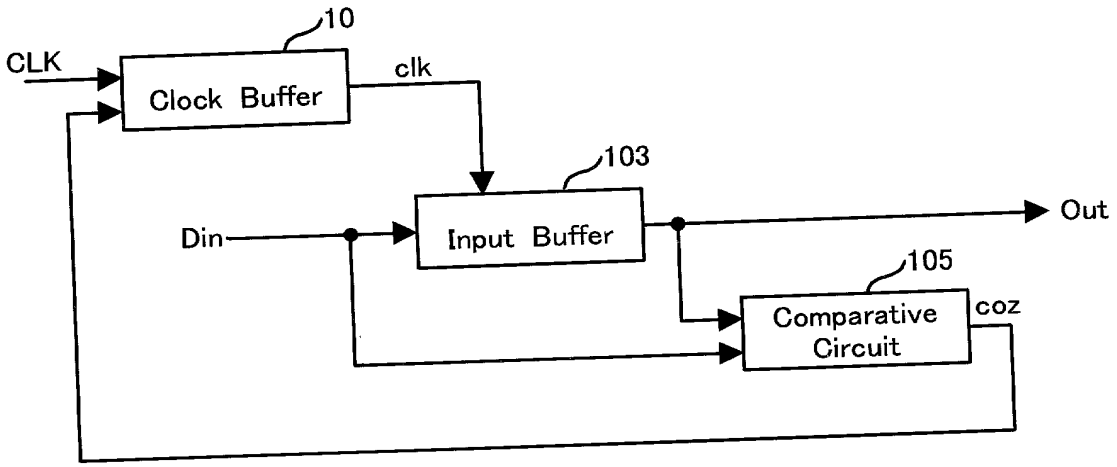
10
CLK
Clock Buffer
clk
103
Din
Input Buffer
Out
105
Comparative Circuit
coz

FIG. 11A

FIG. 11B

FIG. 11C

FIG. 11D

FIG. 11E

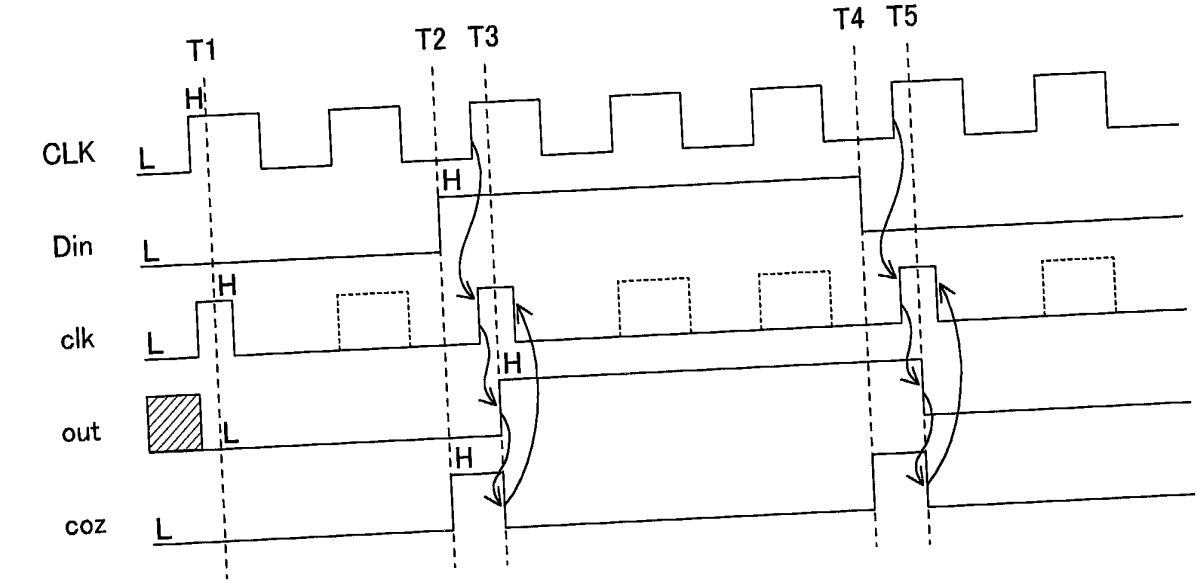

FIG. 12

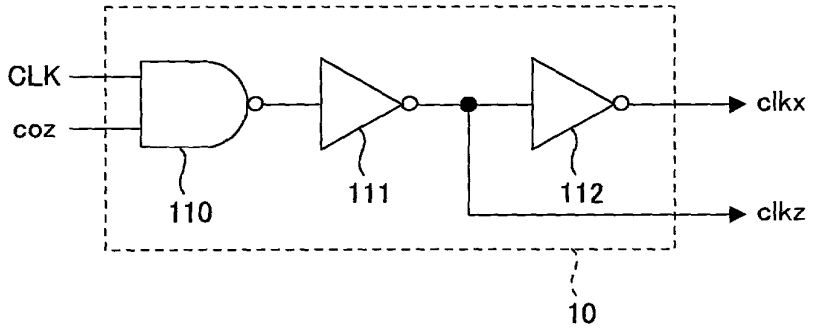
CLK
coz
clkx
clkz
110
111
112
10

FIG. 13

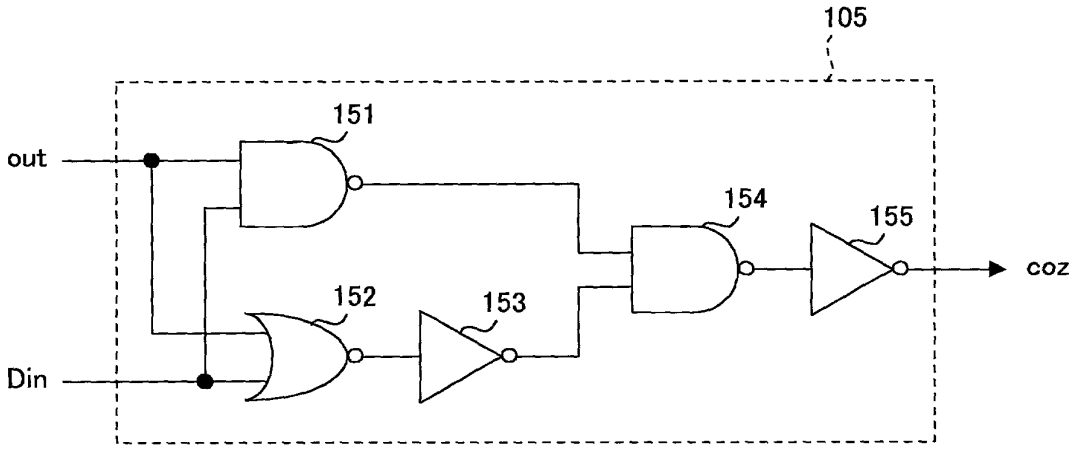
105
151
out
154
155
coz
152
153
Din

FIG. 14

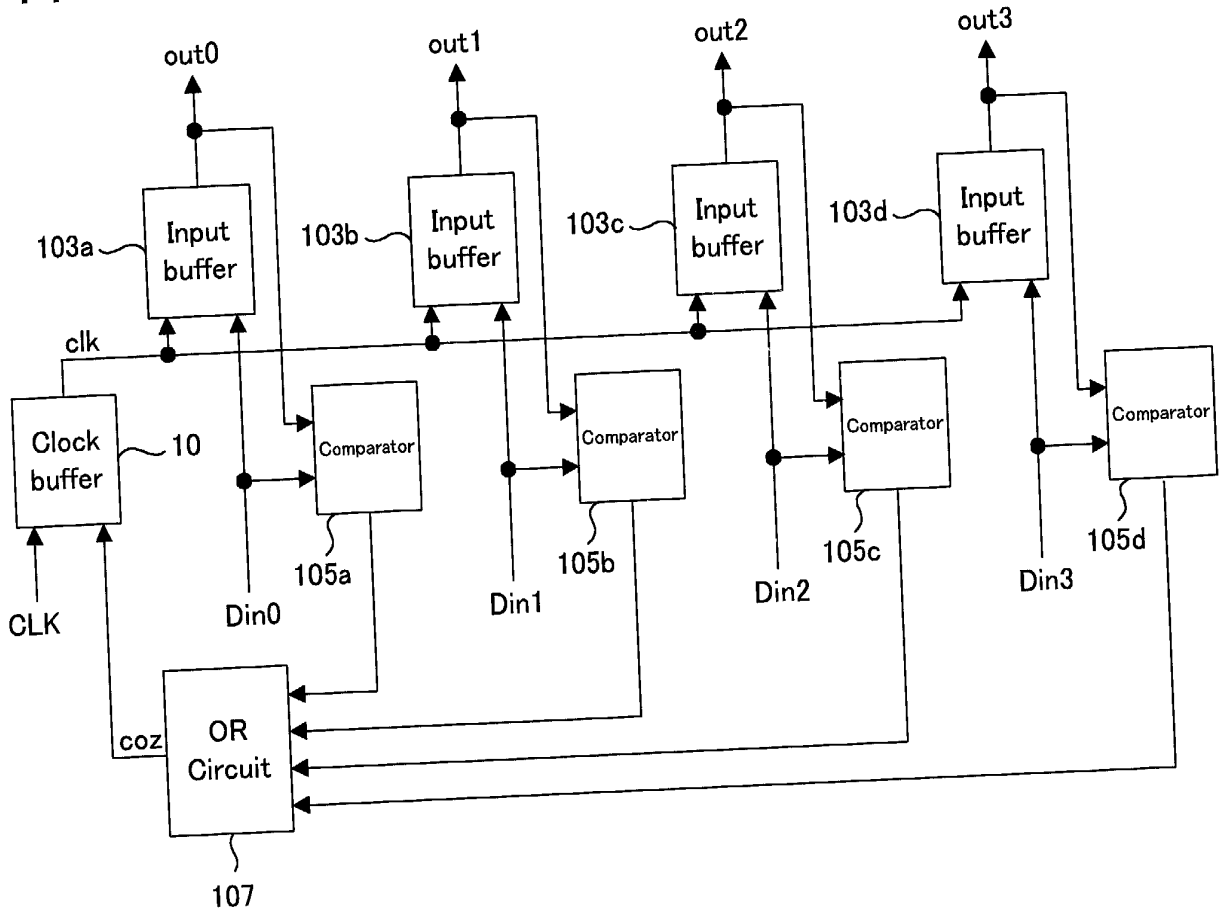
out0
out1
out2
out3
103a
103b
103c
103d
Input buffer
Input buffer
Input buffer
Input buffer
clk
Clock buffer
10
Comparator
Comparator
Comparator
Comparator
105a
105b
105c
105d
CLK
Din0
Din1
Din2
Din3
coz
OR Circuit
107

FIG. 15

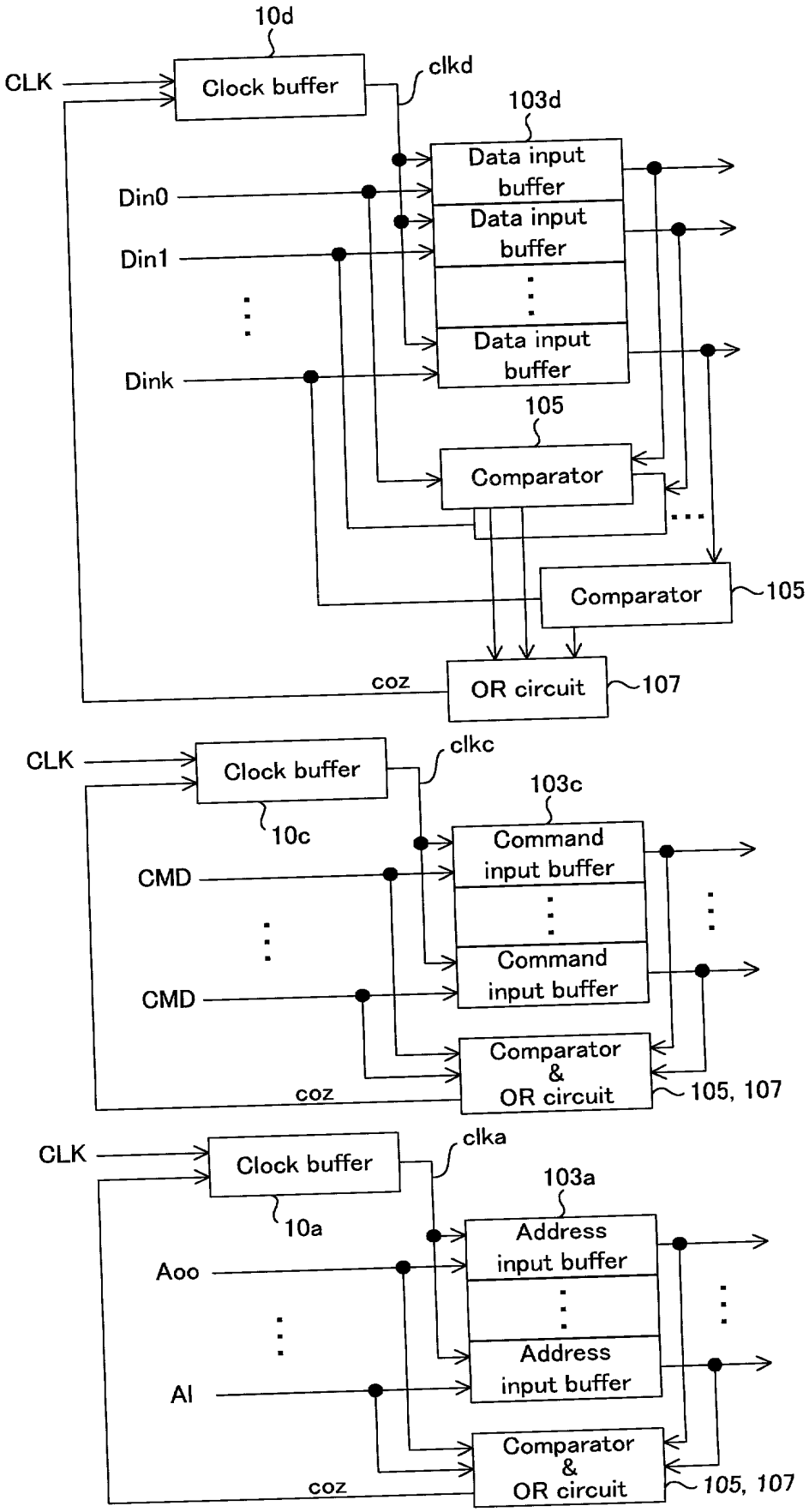
10d
CLK
Clock buffer
clkd
103d
Data input buffer
Din0
Data input buffer
Din1
Data input buffer
Dink
105
Comparator
Comparator
105
coz
OR circuit
107
CLK
Clock buffer
clkc
103c
10c
Command input buffer
CMD
Command input buffer
CMD
Comparator & OR circuit
105, 107
coz
CLK
Clock buffer
clka
103a
10a
Address input buffer
Aoo
Address input buffer
AI
Comparator & OR circuit
105, 107
coz

FIG. 16